Data Sheet

ADM3050E

5.7 kV rms, Signal Isolated, Basic CAN FD Transceiver

FEATURES

- 5.7 kV rms signal isolated CAN FD transceiver
- 1.7 V to 5.5 V supply and logic side levels
- 4.5 V to 5.5 V supply on bus side
- ISO 11898-2:2016-compliant CAN FD
- Data rates up to 12 Mbps for CAN FD
- Low maximum loop propagation delay: 150 ns
- Extended common-mode range: ±25 V
- Bus fault protection (CANH, CANL): ±40 V
- Passes EN 55022, Class B by 6 dB
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 5700 V rms for 1 minute
  - IEC / EN / CSA 62368-1
  - IEC / CSA 61010-1
  - CQC GB 4943.1 (pending)
  - DIN EN IEC 60747-17 (VDE 0884-17) (pending)
    - V_{IORM} = 849 V_{PEAK}
- High common-mode transient immunity: >75 kV/µs
- Industrial operating temperature range: −40°C to +125°C

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Industrial automation
- Process control and building control
- Transport and infrastructure

FUNCTIONAL BLOCK DIAGRAM

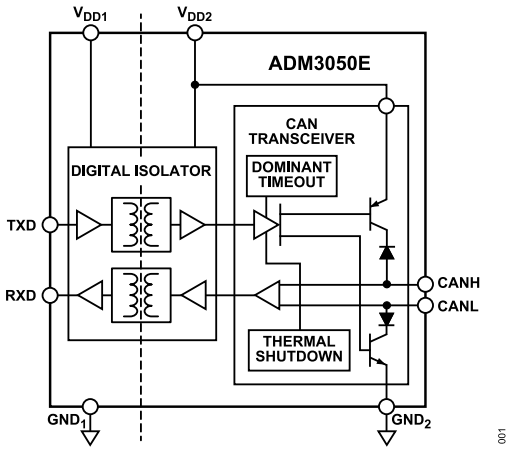

Figure 1.

GENERAL DESCRIPTION

The ADM3050E is a 5.7 kV rms isolated controller area network (CAN) physical layer transceiver with a high performance, basic feature set. The ADM3050E fully meets the CAN flexible data rate (CAN FD) ISO 11898-2:2016 requirements and is further capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 2-channel isolator and a CAN transceiver into a single small outline integrated circuit (SOIC) surface-mount package. The ADM3050E is a fully isolated solution for CAN and CAN FD applications. The ADM3050E provides isolation between the CAN controller and physical layer bus. Safety and regulatory approvals (pending) for a 5.7 kV rms withstand voltage, an 849 V_{PEAK} working voltage, and a 12.8 kV surge test, ensure that the ADM3050E meets application isolation requirements.

Low loop propagation delays and the extended common-mode range of ±25 V support robust communication on longer bus cables.

Dominant timeout functionality protects against bus lock up in a fault condition, and current limiting and thermal shutdown features protect against output short circuits. The CAN bus input and output pins are protected to ±40 V against accidental connection to a +24 V bus supply. The device is fully specified over the −40°C to +125°C industrial temperature range.

Rev. C

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REVISION HISTORY

10/2024—Rev. B to Rev. C

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SPECIFICATIONS

All voltages are relative to their respective ground, 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Bus Side	I_{DD2}					
Recessive State			5.3	7	mA	TXD high, load resistance (R_L) = 60 Ω
Dominant State			63	75	mA	Limited by transmit dominant timeout (t_{DT}), see the Theory of Operation section, R_L = 60 Ω
				73	mA	Limited by t_{DT}, R_L = 60 Ω, 4.75 V ≤ V_{DD2} ≤ 5.25 V
70% Dominant/30% Recessive						Worst case, see the Theory of Operation section, R_L = 60 Ω
1 Mbps			45	58	mA	
5 Mbps			49	60	mA	
12 Mbps			58	65	mA	
Logic Side *i*Coupler Current	I_{DD1}			5.5	mA	TXD high, low, or switching
DRIVER						
Differential Outputs						See Figure 20
Recessive State Voltage						TXD high, R_L, and common-mode filter capacitor (C_F) open
CANH, CANL	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output	V_{OD}	−500		+50	mV	
Dominant State Voltage						TXD low, C_F open
CANH	V_{CANH}	2.75		4.5	V	50 Ω ≤ R_L ≤ 65 Ω
CANL	V_{CANL}	0.5		2.0	V	50 Ω ≤ R_L ≤ 65 Ω
Differential Output	V_{OD}	1.5		3.0	V	50 Ω ≤ R_L ≤ 65 Ω
		1.4		3.3	V	45 Ω ≤ R_L ≤ 70
		1.5		5.0	V	R_L = 2240 Ω
Output Symmetry (V_{DD2} − V_{CANH} to V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60 Ω, C_F = 4.7 nF
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3 V
CANL				115	mA	V_{CANL} = 18 V
Steady State						
CANH				115	mA	V_{CANH} = −24 V
CANL				115	mA	V_{CANL} = 24 V
Logic Input TXD						
Input Voltage						
High	V_{IH}	0.65 × V_{DD1}			V	
Low	V_{IL}			0.35 × V_{DD1}	V	
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	µA	Input high or low
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 21, RXD capacitance (C_{RXD}) open, −25 V < V_{CANL}, V_{CANH} < +25 V
Recessive		−1.0		+0.5	V	
Dominant		0.9		5.0	V	
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\|I_{IN\ (OFF)}\|$			10	µA	V_{CANH}, V_{CANL} = 5 V, V_{DD2} = 0 V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Resistance						
CANH, CANL	R_{INH}, R_{INL}	6		25	kΩ	
Differential	R_{DIFF}	20		100	kΩ	
Input Resistance Matching	m_R	−0.03		+0.03		$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
CANH, CANL Input Capacitance	C_{INH}, C_{INL}		35		pF	
Differential Input Capacitance	C_{DIFF}		12		pF	
Logic Output (RXD)						
Output Voltage						
Low	V_{OL}		0.2	0.4	V	Output impedance (I_{OUT}) = 2 mA
High	V_{OH}	V_{DD1} − 0.2			V	I_{OUT} = −2 mA
Short-Circuit Current	I_{OS}	7		85	mA	Output voltage (V_{OUT}) = GND_1 or V_{DD1}
COMMON-MODE TRANSIENT IMMUNITY[1]						Common-mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V
Input High, Recessive	$\|CM_H\|$	75	100		kV/µs	Input voltage (V_{IN}) = V_{DD1} (TXD) or CANH/CANL recessive
Input Low, Dominant	$\|CM_L\|$	75	100		kV/µs	V_{IN} = 0 V (TXD) or CANH/CANL dominant

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL recessive or RXD ≥ V_{DD1} − 0.2 V. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL dominant or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground, 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						See Figure 2 and Figure 20, t_{BIT_TXD} = 200 ns, R_L = 60 Ω, C_L = 100 pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		45	70	ns	
Transmit Dominant Timeout	t_{DT}	1175		4000	µs	TXD low, see Figure 3
RECEIVER						See Figure 2 and Figure 22, t_{BIT_TXD} = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}			150	ns	
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}			150	ns	
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2 Mbps		450		550	ns	t_{BIT_TXD} = 500 ns
5 Mbps		160		220	ns	t_{BIT_TXD} = 200 ns
8 Mbps		85		140	ns	t_{BIT_TXD} = 125 ns
12 Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3 ns

SPECIFICATIONS

TIMING DIAGRAMS

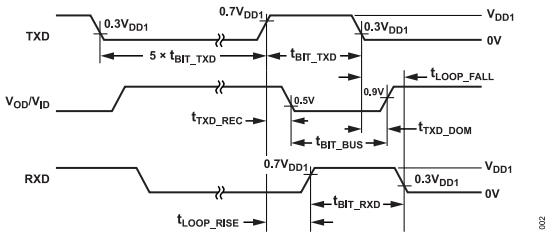

Figure 2. Transceiver Timing Diagram

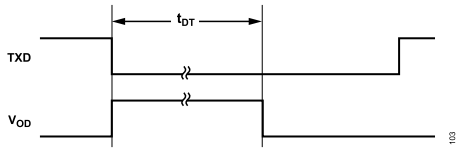

Figure 3. Dominant Timeout, t_{DT}

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value		Unit	Test Conditions/Comments
		ADM3050EBRWZ	ADM3050EBRIZ		
Rated Dielectric Insulation Voltage		5700	5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L (I01)	7.8	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB) Clearance	L (PCB)	7.8	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	29	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)[3]	CTI	>600	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I	I		Material group per IEC 60664-1

1 In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 meters.

2 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

3 CTI rating for the ADM3050E is >600 V and Material Group I isolation group.

SPECIFICATIONS

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.1		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	

[1] The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

ADM3050EBRWZ

The ADM3050EBRWZ certification approvals are listed in Table 5.

Table 5.

UL	CSA	VDE (Pending)	CQC
UL1577[1]	IEC / EN / CSA 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)[2]	Certified under CQC11-471543-2012
Single Protection, 5700 V rms	Basic Insulation, 830 V rms	Reinforced insulation, 849 V_{PEAK}	CQC GB4943.1
	Reinforced Insulation, 415 V rms		Basic insulation, 780 V rms
	IEC / CSA 60601-1		Reinforced insulation, 390 V rms
	Reinforced Insulation (2 MOPP), 237.5 V rms		
	IEC / CSA 61010-1		
	Basic Insulation, 600 V rms, overvoltage category IV		
	Reinforced Insulation, 300 V rms		
File E214100	File No. 205078	Certificate No: (Pending)	Certificate No. CQC19001229559

[1] In accordance with UL 1577, each ADM3050E is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each product is proof tested by applying an insulation test voltage ≥ 1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

ADM3050EBRIZ

The ADM3050EBRIZ certification approvals are listed in Table 6.

Table 6.

UL	CSA	VDE (Pending)	CQC (Pending)
UL1577[1]	IEC / EN / CSA 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)[2]	Certified under CQC11-471543-2012
Single Protection, 5700 V rms	Basic Insulation, 830 V rms	Reinforced insulation, 849 V_{PEAK}	CQC GB4943.1
	Reinforced Insulation, 415 V rms		Basic insulation, 780 V rms
	IEC / CSA 60601-1		Reinforced insulation, 390 V rms
	Reinforced Insulation (2 MOPP), 261 V rms		
	IEC / CSA 61010-1		
	Basic Insulation, 600 V rms, overvoltage category IV		
	Reinforced Insulation, 300 V rms		
File E214100	File No. 205078	Certificate No: (pending)	Certificate (pending)

SPECIFICATIONS

[1] In accordance with UL 1577, each ADM3050E is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each product is proof tested by applying an insulation test voltage ≥ 1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 7. ADM3050EBRWZ VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	849	V_{PEAK}
Maximum Working Insulation Voltage		V_{IOWM}	600	V_{RMS}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{pd\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1358	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1019	V_{PEAK}
Maximum Transient Isolation Voltage		V_{IOTM}	8000	V_{PEAK}
Maximum Impulse Voltage	Tested in air, 1.2µs/50µs waveform per IEC 61000-4-5	V_{IMP}	8000	V_{PEAK}
Maximum Surge Isolation Voltage	Tested in oil, 1.2µs/50µs waveform per IEC 61000-4-5, V_{TEST} = V_{IMP} × 1.3 or ≥ 10kV	V_{IMP}	12800	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.08	W
Insulation Resistance at T_S	Test voltage = 500 V	R_S	$>10^9$	Ω

Table 8. ADM3050EBRIZ VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	849	V_{PEAK}
Maximum Working Insulation Voltage		V_{IOWM}	600	V_{RMS}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{pd\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1358	V_{PEAK}

SPECIFICATIONS

Table 8. ADM3050EBRIZ VDE Characteristics (Continued)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1019	V_{PEAK}
Maximum Transient Isolation Voltage		V_{IOTM}	8000	V_{PEAK}
Maximum Impulse Voltage	Tested in air, 1.2µs/50µs waveform per IEC 61000-4-5	V_{IMP}	8000	V_{PEAK}
Maximum Surge Isolation Voltage	Tested in oil, 1.2µs/50µs waveform per IEC 61000-4-5, $V_{TEST} = V_{IMP} \times 1.3$ or ≥ 10kV	V_{IMP}	12800	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.28	W
Insulation Resistance at T_S	Test voltage = 500 V	R_S	$>10^9$	Ω

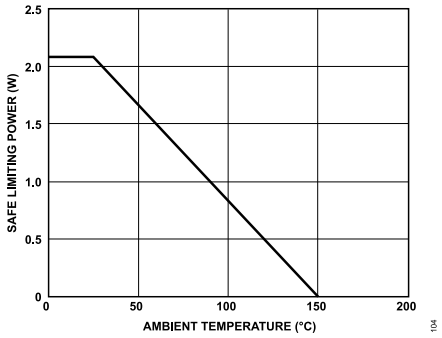

Figure 4. ADM3050EBRWZ Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17) (See the Thermal Resistance Section for Additional Information)

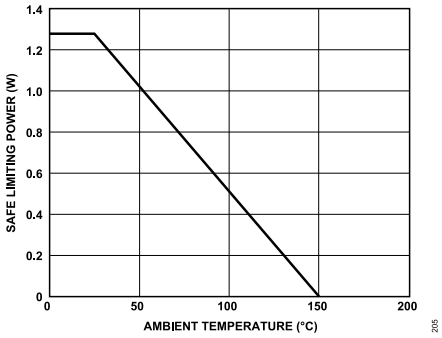

Figure 5. ADM3050EBRIZ Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17) (See the Thermal Resistance Section for Additional Information)

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to GND_1/GND_2 are on same side, unless otherwise noted.

Table 9.

Parameter	Rating
V_{DD1}/V_{DD2}	−0.5 V to +6 V
Logic Side Input and Output: TXD, RXD	−0.5 V to V_{DD1} + 0.5 V
CANH, CANL	−40 V to +40 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_J)	150°C
Electrostatic Discharge (ESD), IEC 61000-4-2, CANH/CANL	
Across Isolation Barrier with Respect to GND_1	±8 kV
Contact Discharge with Respect to GND_2	±8 kV typical
Air Discharge with Respect to GND_2	±15 kV
Human Body Model (HBM), All Pins, 1.5 kΩ, 100 pF	±4 kV
Moisture Sensitivity Level (MSL)	3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 10. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
RW-16	60	°C/W
RI-8-1	97	°C/W

[1] The thermocouple is located at the center of the package underside, and the test was conducted on a 4-layer board with thin traces. See the Thermal Analysis section for the thermal model definitions.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

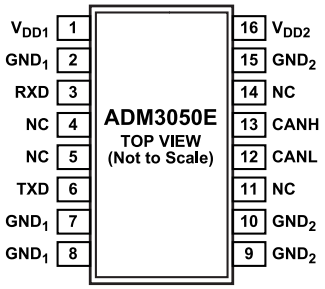

Figure 6. 16-Lead SOIC_W Pin Configuration

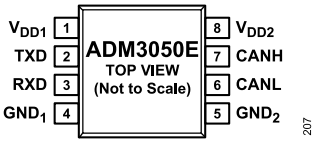

Figure 7. 8-Lead SOIC_IC Pin Configuration

Table 11. Pin Function Descriptions

Pin No.			
16-Lead SOIC_W	8-Lead SOIC_IC	Mnemonic	Description
1	1	V_{DD1}	Power Supply, Logic Side, 1.7 V to 5.5 V. This pin requires a 0.1 µF decoupling capacitor.
2, 7, 8	4	GND_1	Ground, Logic Side.
3	3	RXD	Receiver Output Data.
4, 5, 11, 14	N/A[1]	NC	No Connect. No internal connection to IC.
6	2	TXD	Driver Input Data.
9, 10, 15	5	GND_2	Ground, Bus Side.
12	6	CANL	CAN Low Input and Output.
13	7	CANH	CAN High Input and Output.
16	8	V_{DD2}	Power Supply, Bus Side, 4.5 V to 5.5 V. This pin requires a 0.1 µF decoupling capacitor.

[1] N/A means not applicable.

OPERATIONAL TRUTH TABLE

Table 12. Truth Table

V_{DD1}	V_{DD2}	TXD	Mode	RXD	CANH/CANL
On	On	Low	Normal	Low	Dominant (limited by t_{DT})
On	On	High	Normal	High per bus	Recessive and set by bus
Off	On	Don't care	Normal	Indeterminate	Recessive and set by bus
On	Off	Don't care	Transceiver off	High	High-Z

TYPICAL PERFORMANCE CHARACTERISTICS

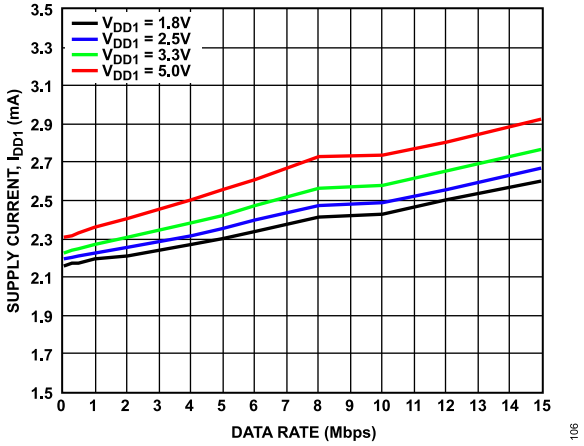

Figure 8. Supply Current (I_{DD1}) vs. Data Rate

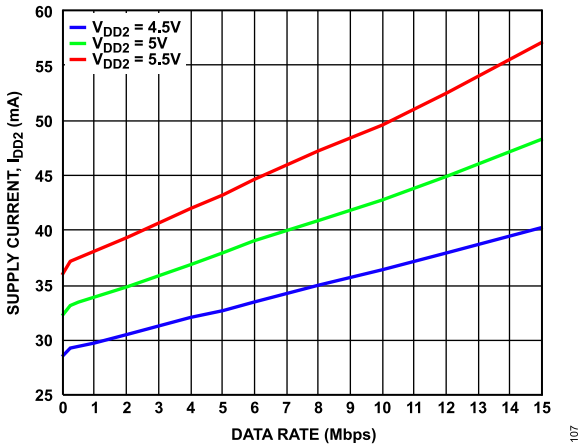

Figure 9. Supply Current (I_{DD2}) vs. Data Rate

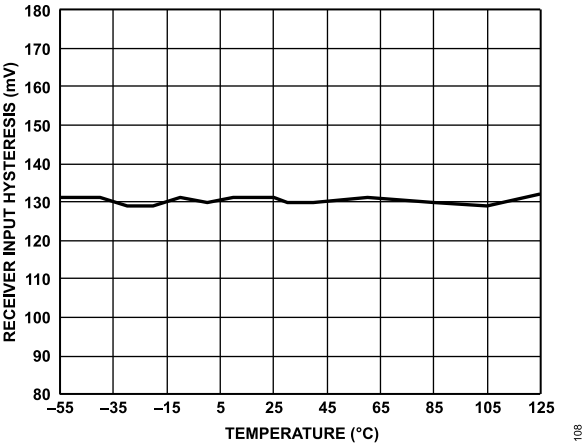

Figure 10. Receiver Input Hysteresis vs. Temperature

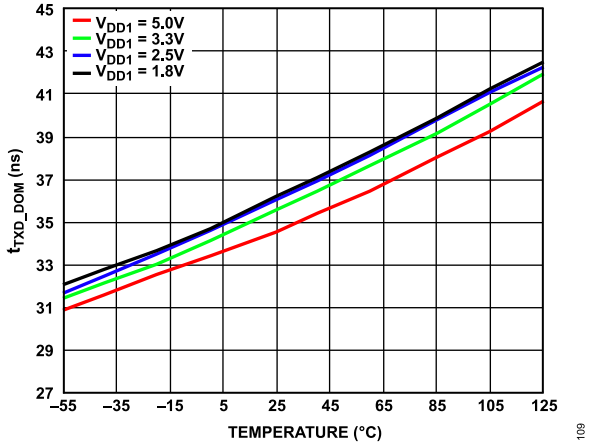

Figure 11. t_{TXD_DOM} vs. Temperature

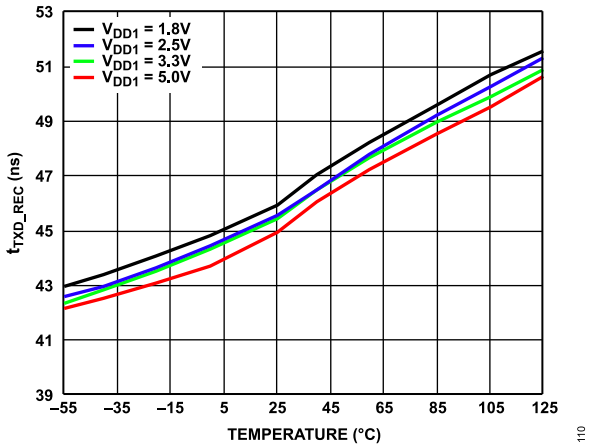

Figure 12. t_{TXD_REC} vs. Temperature

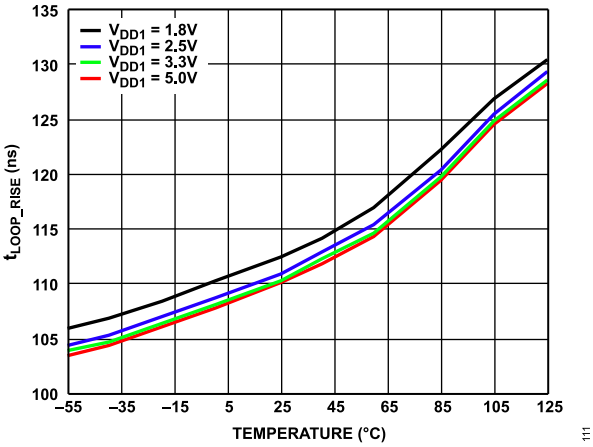

Figure 13. t_{LOOP_RISE} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

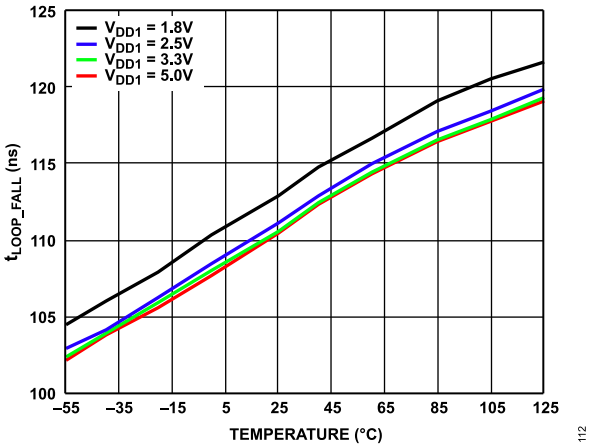

Figure 14. t_{LOOP_FALL} vs. Temperature

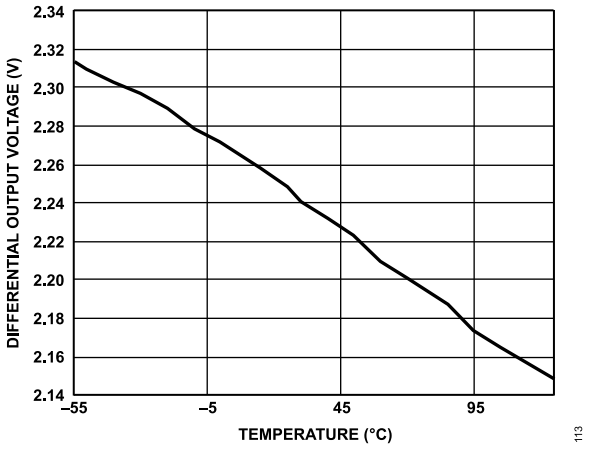

Figure 15. Differential Output Voltage vs. Temperature, R_L = 60 Ω

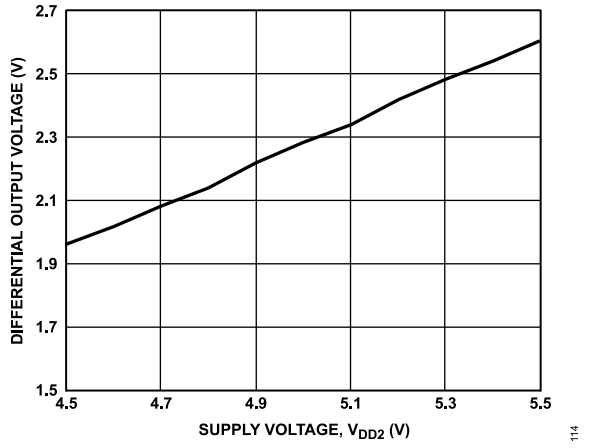

Figure 16. Differential Output Voltage vs. Supply Voltage (V_{DD2}), R_L = 60 Ω

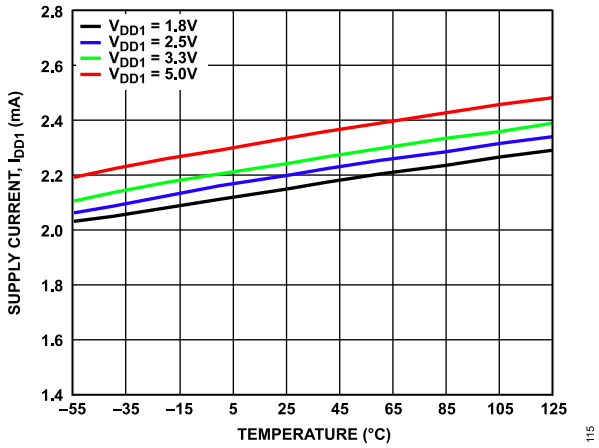

Figure 17. Supply Current (I_{DD1}) vs. Temperature

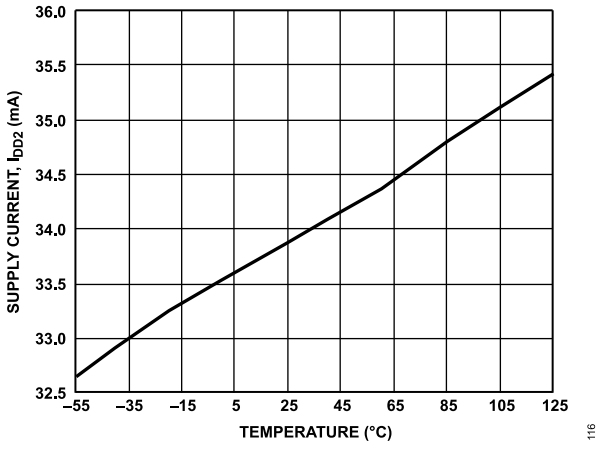

Figure 18. Supply Current (I_{DD2}) vs. Temperature

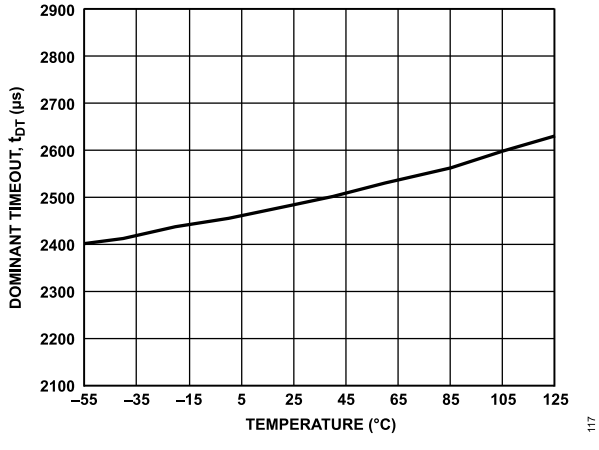

Figure 19. Dominant Timeout (t_{DT}) vs. Temperature

TEST CIRCUITS

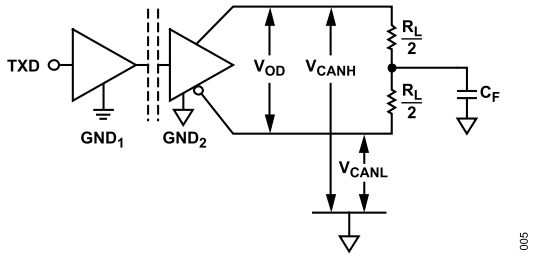

Figure 20. Driver Voltage Measurement

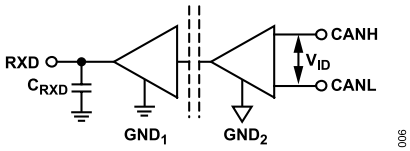

Figure 21. Receiver Voltage Measurement

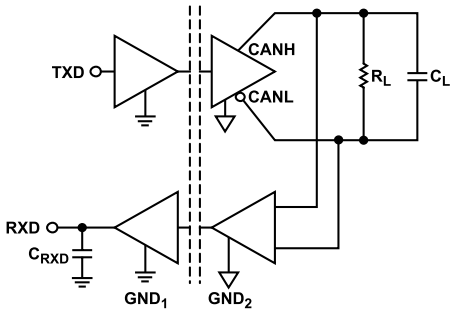

Figure 22. Switching Characteristics Measurements

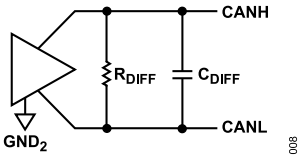

Figure 23. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

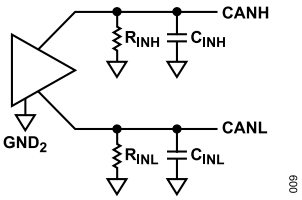

Figure 24. Input Resistance (R_{INx}) and Input Capacitance (C_{INx}) Measured in Recessive State, Bus Disconnected

TERMINOLOGY

I_{DD1}

I_{DD1} is the current drawn by the V_{DD1} pin.

I_{DD2}

I_{DD2} is the current drawn by the V_{DD1} pin.

V_{OD} and V_{ID}

V_{OD} and V_{ID} are the differential voltages from the transmitter or at the receiver on the CANH and CANL pins.

t_{TXD_DOM}

t_{TXD_DOM} is the propagation delay from a low signal on TXD to transition the bus to a dominant state.

t_{TXD_REC}

t_{TXD_REC} is the propagation delay from a high signal on TXD to transition the bus to a recessive state.

t_{LOOP_FALL}

t_{LOOP_FALL} is the propagation delay of a low signal on the TXD pin to the bus dominant. t_{ON_LOOP} transitions low on the RXD pin.

t_{LOOP_RISE}

t_{LOOP_RISE} is the propagation delay of a high signal on TXD to the bus recessive. t_{OFF_LOOP} transitions high on the RXD pin.

t_{BIT_TXD}

t_{BIT_TXD} is the bit time at the TXD pin as transmitted by the CAN controller. See Figure 2 for level definitions.

t_{BIT_BUS}

t_{BIT_BUS} is the bit time as transmitted by the transceiver to the bus. When compared with a given t_{BIT_TXD}, a measure of bit symmetry from the TXD digital isolation channel and CAN transceiver can be determined. See Figure 2 for level definitions.

t_{BIT_RXD}

t_{BIT_RXD} is the bit time on the RXD output pin, which can be compared with t_{BIT_TXD} for a round trip measure of pulse width distortion through the TXD digital isolation channel, the CAN transceiver, and back through the RXD isolation channel.

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

The ADM3050E facilitates communication between a CAN controller and the CAN bus. The CAN controller and the ADM3050E communicate with standard 1.8 V, 2.5 V, 3.3 V or 5.0 V CMOS levels. The internal transceiver translates the CMOS levels to and from the CAN bus.

The CAN bus has two states: dominant and recessive. The recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. In the recessive state, both the CANH pin and CANL pin are set to high impedance and are loosely biased to a single-ended voltage of 2.5 V. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 1.5 V. The transceiver transmits a dominant state by driving the single-ended voltage of the CANH line to 3.5 V and the CANL pin to 1.5 V. The recessive and dominant states correspond to CMOS high and CMOS low, respectively, on the RXD pin and TXD pin.

A dominant state from another node overwrites a recessive state on the bus. A CAN frame can be set for higher priority by using a longer string of dominant bits to gain control of the CAN bus during the arbitration phase. While transmitting, a CAN transceiver also reads back the state of the bus. When a CAN controller receives a dominant state while transmitting a recessive state during arbitration, the CAN controller surrenders the bus to the node still transmitting the dominant state. The node that gains control during the arbitration phase reads back only its own transmission. This interaction between recessive and dominant states allows competing nodes to negotiate for control of the bus while avoiding contention between nodes.

Industrial applications can have long cable runs. These long runs may have differences in local earth potential. Different sources may also power nodes. The ADM3050E transceiver has a ±25 V common-mode range (CMR) that exceeds the ISO11898-2 requirement and further increases the tolerance to ground variation.

See the AN-1123 Application Note for additional information on CAN.

SIGNAL ISOLATION

The ADM3050E device provides galvanic signal isolation implemented on the logic side of the interface. The RXD and TXD channels are isolated using a low propagation delay on/off keying (OOK) architecture with *i*Coupler digital isolation technology.

The low propagation delay isolation, quick transceiver conversion speeds, and integrated form factor are critical for longer cable lengths, higher data speeds, and reducing the total solution board space. The ADM3050E isolated transceiver reduces solution board space while increasing data transfer rates over discrete optocoupler and transceiver solutions.

INTEGRATED AND CERTIFIED IEC ELECTROMAGNETIC COMPATIBILITY (EMC) SOLUTION

Typically, designers must add protections against harsh operating environments while also making the product as small as possible. To reduce the board space and the design efforts needed to meet system level ESD standards, the ADM3050E isolated transceiver has brought robust protection circuitry on-chip for the CANH and CANL lines.

±40 V MISWIRE PROTECTION

High voltage miswire events commonly occur when the system power supply is connected directly to the CANH and the CANL bus lines during assembly. Supplies may also be shorted by accidental damage to the field bus cables while the system is operating. Accounting for inductive kick and switching effects, the ADM3050E isolated transceiver CAN bus lines are protected against these miswire or shorting events in systems with up to nominal 24 V supplies. The CANH and CANL signal lines can withstand a continuous supply short with respect to GND_2 or between the CAN bus lines without damage. This level of protection applies when the device is either powered or unpowered.

DOMINANT TIMEOUT

The ADM3050E features a dominant timeout (t_{DT} in Figure 3). A TXD line shorted to ground, or malfunctioning CAN controller are examples of how a single node can indefinitely prevent further bus traffic. t_{DT} limits how long the dominant state can transmit to the CAN bus by the transceiver. The TXD function restores when the line is presented with a logic low.

The t_{DT} minimum also inherently creates a minimum data rate. Under normal operation, the CAN protocol allows five consecutive bits of the same polarity before stuffing a bit of opposite polarity into the transmitting bit sequence. When an error is detected, the CAN controller purposely violates the bit stuffing rules by producing six consecutive dominant bits. At any given data rate, the CAN controller must transmit as many as 11 consecutive dominant bits to effectively limit the ADM3050E minimum data rate to 9600 bps.

FAIL-SAFE FEATURES

In cases where the TXD input pin is allowed to float to prevent bus traffic interruption, the TXD input channel has an internal pull-up to the V_{DD1} pin. The pull-up holds the transceiver in the recessive state.

THERMAL SHUTDOWN

The integrated transceiver is designed with thermal shutdown circuitry to protect the device from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. The circuitry disables the driver

THEORY OF OPERATION

outputs when the die temperature reaches 175°C. The drivers are enabled after the die has cooled.

APPLICATIONS INFORMATION

RADIATED EMISSIONS AND PCB LAYOUT

The ADM3050E isolated CAN transceivers with integrated dc-to-dc converters pass EN 55022, Class B by 6 dB on a simple 2-layer PCB design. Neither stitching capacitance nor high voltage surface mount (SMT) safety capacitors are required to meet this emission level.

PCB LAYOUT

The ADM3050E isolated CAN transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the logic input supply (V_{DD1}), and the shared CAN transceiver and digital isolator supply pin (V_{DD2}). The recommended bypass capacitor value is 0.1 µF. Note that low effective series resistance (ESR) bypass capacitors are required and must be placed as close to the chip pads as possible. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1, Pin 7, and Pin 8 and between Pin 16, Pin 10, and Pin 9 must also be considered, unless the ground pair on each package side is connected in close proximity to the package.

In applications involving high common-mode transients, minimize board coupling across the isolation barrier. Design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this equal coupling can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

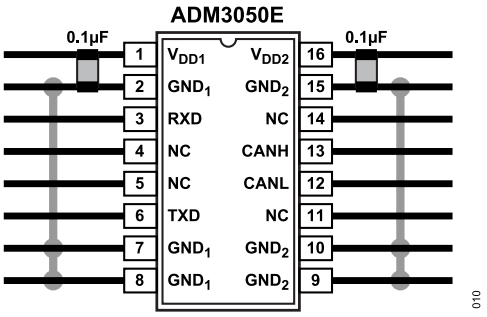

Figure 25. Recommended 16-Lead SOIC_W PCB Layout

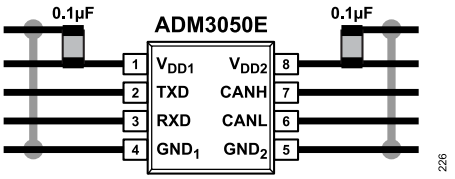

Figure 26. Recommended 8-Lead SOIC_IC PCB Layout

THERMAL ANALYSIS

The ADM3050E device consists of three internal die attached to a split lead frame. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} value from Table 10. The θ_{JA} value is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RW-16	SOIC_W	16-Lead Standard Small Outline Package
RI-8-1	SOIC_IC	8-Lead Standard Small Outline Package, with Increased Creepage

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3050EBRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM3050EBRWZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM3050EBRIZ	−40°C to +125°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
ADM3050EBRIZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Package Description
EVAL-ADM3050EEBZ	Evaluation Board

[1] Z = RoHS Compliant Part.